UG-2828GDEDF11

Application note

Evaluation Kit User Guide

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Version: Preliminary

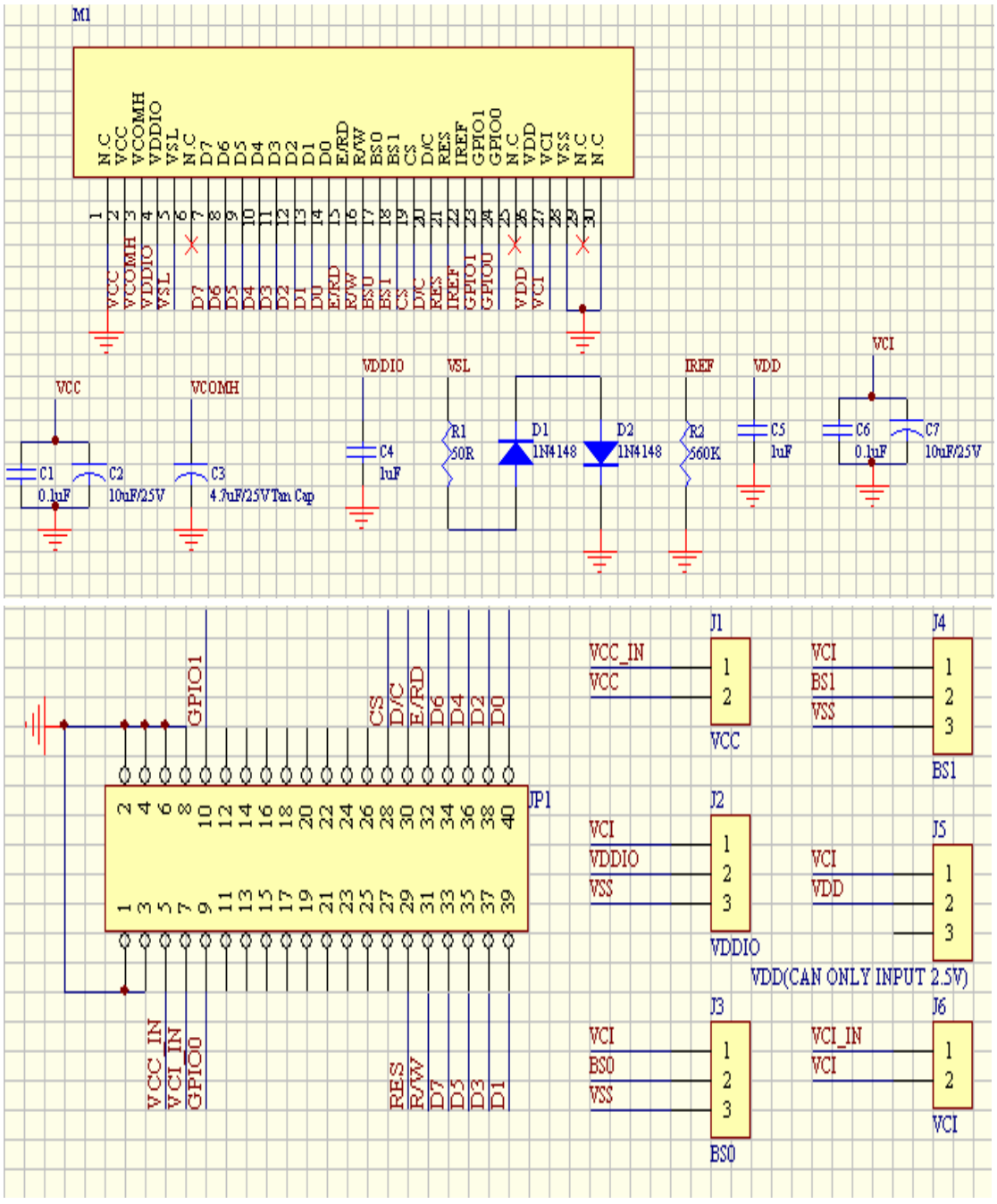
Contents

1. REVISION HISTORY

Date	Page	Contents	Version
2008/10/06	*	Preliminary	Preliminary 1.0

2. Schematic

2.1 EVK Schematic



3. Symbol define

D0-D7：These pins are bi-directional data bus connecting to the MCU data bus. For SPI application, D[0]=SCLK & D[1]=SDIN.

Unused pins are recommended to tie LOW except D[2].

BS0,BS1,BS2,BS3：MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS3 and BS2 are command programmable (by command ABh).[reset = 00]. BS1 and BS0 are pin select (J3, J4).

Regarding to the application of BS3 and BS2, they should be fixed as 00.

BS[3:0]	Interface
XX00	4 line SPI
XX01	3 line SPI
0011	8-bit 6800 parallel
0010	8-bit 8080 parallel

Table 1 – MCU Interface Selection Setting

E (RD#)：This pin is MCU interface input.

When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.

When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.

When serial interface is selected, this pin E(RD#) must be connected to V_{SS}.

R/W#：This pin is read / write control input pin connecting to the MCU interface.

When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.

When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.

When serial interface is selected, this pin R/W (WR#) must be connected to V_{SS}.

D/C#：This pin is Data/Command control pin connecting to the MCU.

When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data.

When the pin is pulled LOW, the data at D[7:0] will be interpreted as command.
4-Wire SPI Interface D/C pin Data/Command control pin connecting to the MCU.
3-Wire SPI Interface D/C pin Tie Low.

RES#：This pin is reset signal input.
When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.

CS#：This pin is the chip select input connecting to the MCU.
The chip is enabled for MCU communication only when CS# is pulled LOW.

VCC：Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.

VCI：Low voltage power supply

GND：Power supply ground.

VDDIO：Power supply for interface logic level. It should match with the MCU interface voltage level and must be connected to external source.

VSL：This is segment voltage reference pin.
When external VSL is not used, this pin should be left open.
When external VSL is used, connect with resistor and diode to ground. (details depend on application)

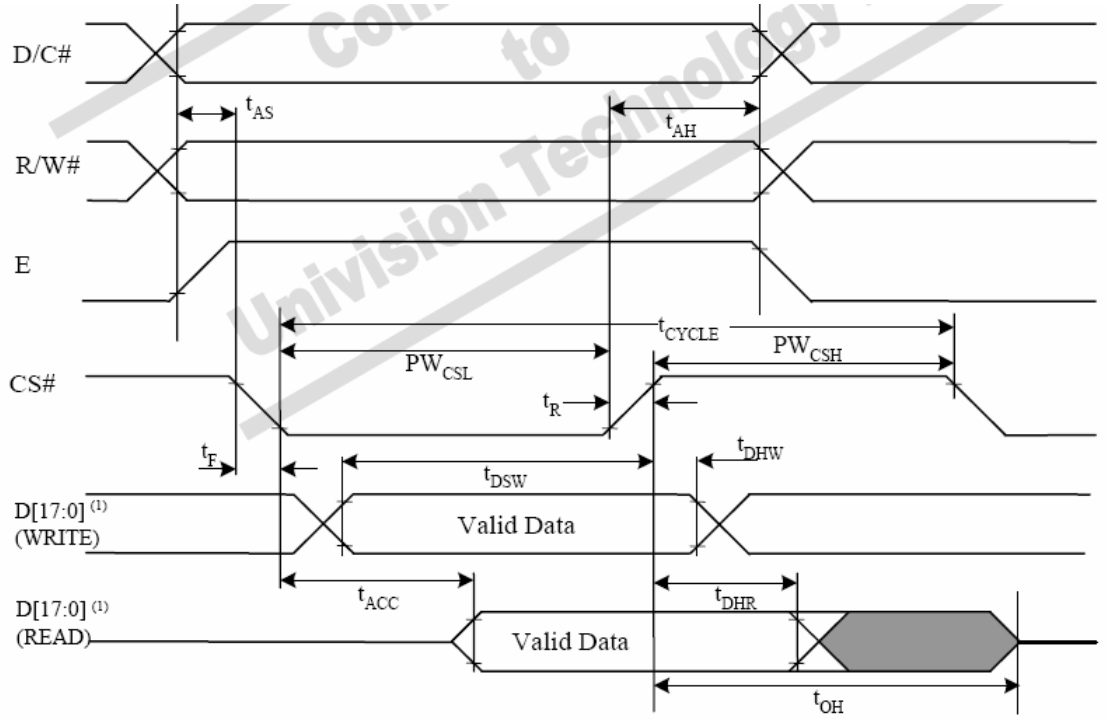
V_{COMH}：COM signal deselected voltage level.
A capacitor should be connected between this pin and V_{SS}.

GPIO0: Detail refer to Command B5h

GPIO1: Detail refer to Command B5h

4. TIMMING CHARACTERISTICS

4.1 6800-Series MPU parallel Interface



Note
(1) when 8 bit used: D[7:0] instead; when 16 bit used: D[15:0] instead; when 18 bit used: D[17:0] instead.

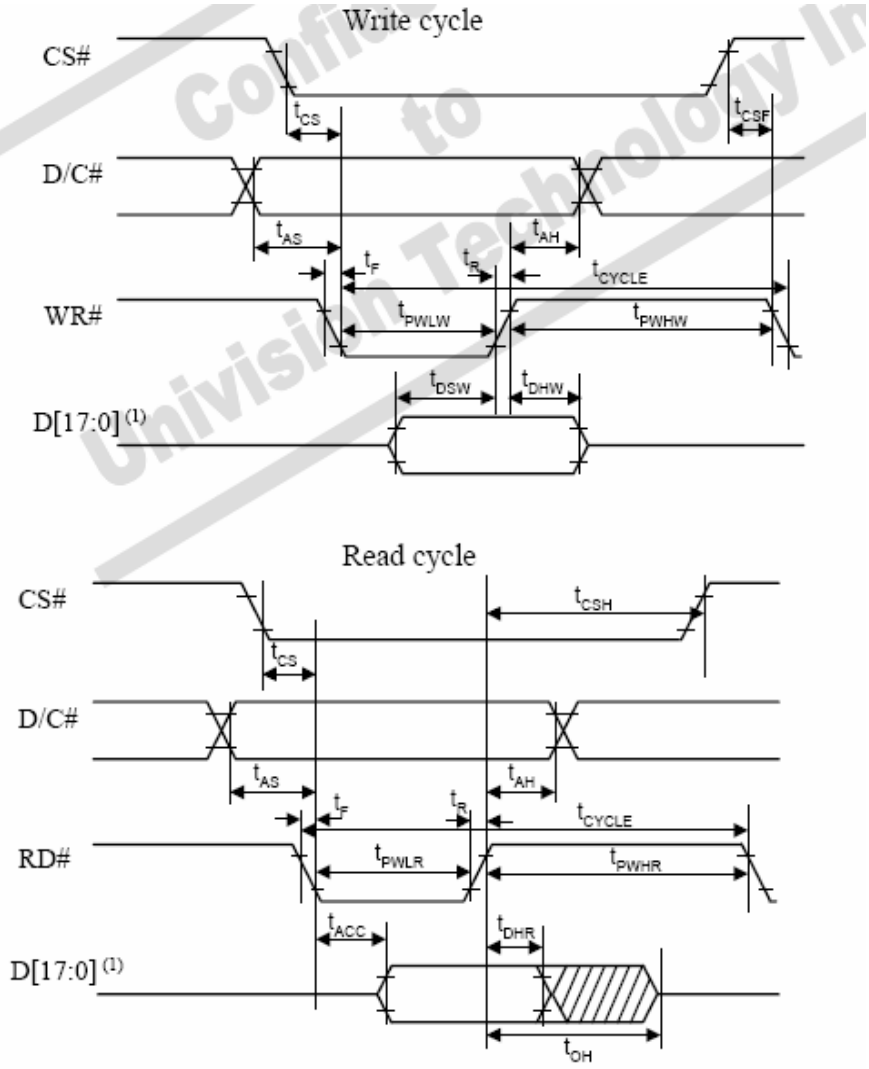
Figure 1 6800-series MCU parallel interface characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.65V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 2 6800-Series MCU Parallel Interface Timing Characteristics

4.2 8080-Series MPU parallel Interface



Note
(1) when 8 bit used: D[7:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.

Figure 2 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.65V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Table 3 8080-Series MPU parallel Interface Timing Characteristics

4.3 4-Wire SPI Interface

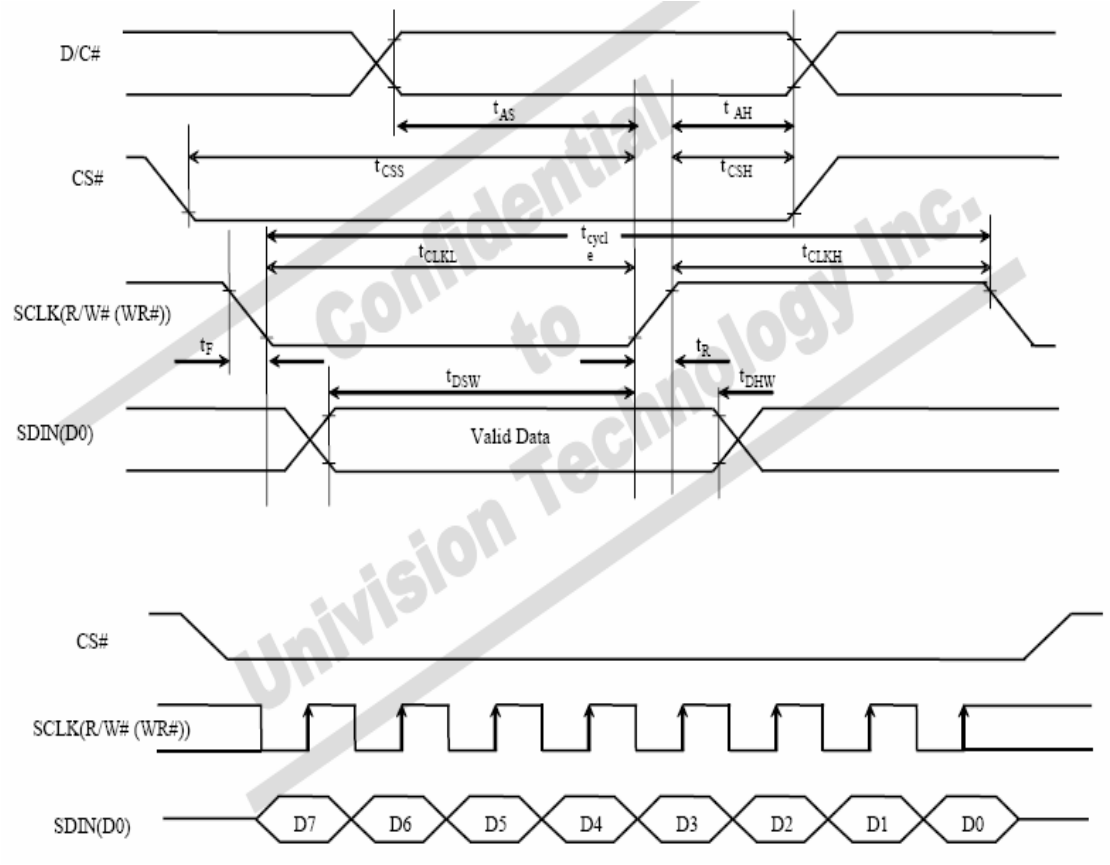


Figure 3 Serial interface characteristics (4-wire SPI)

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.65V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 4 Serial Interface Timing Characteristics (4-wire SPI)

4.4 3- Wire SPI Interface

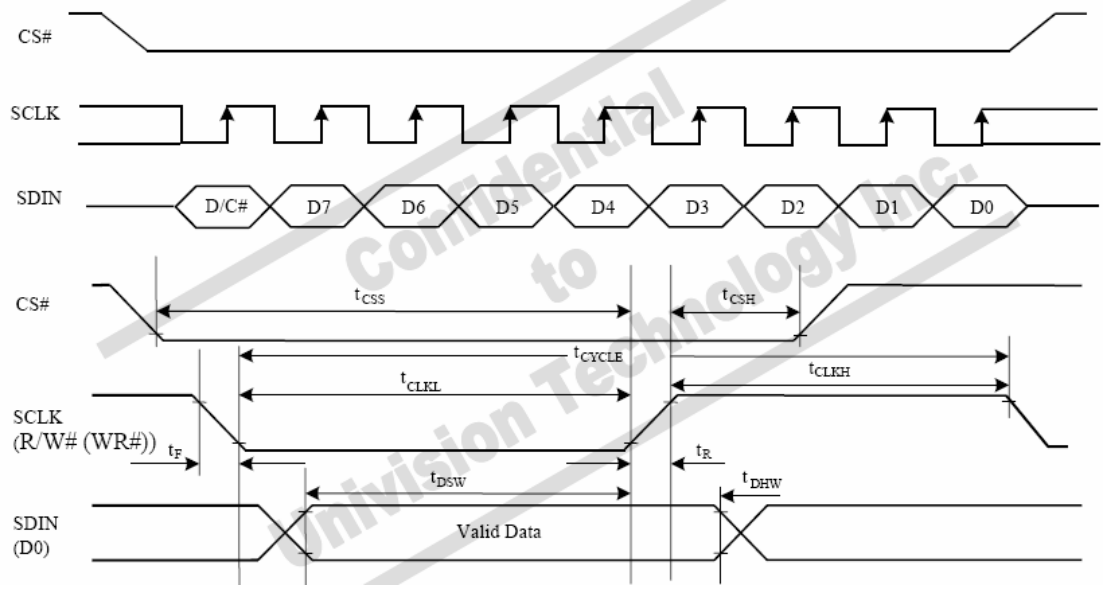


Figure 4 Serial interface characteristics (3-wire SPI)

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.65V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 5 Serial Interface Timing Characteristics (3-wire SPI)

5. EVK use introduction

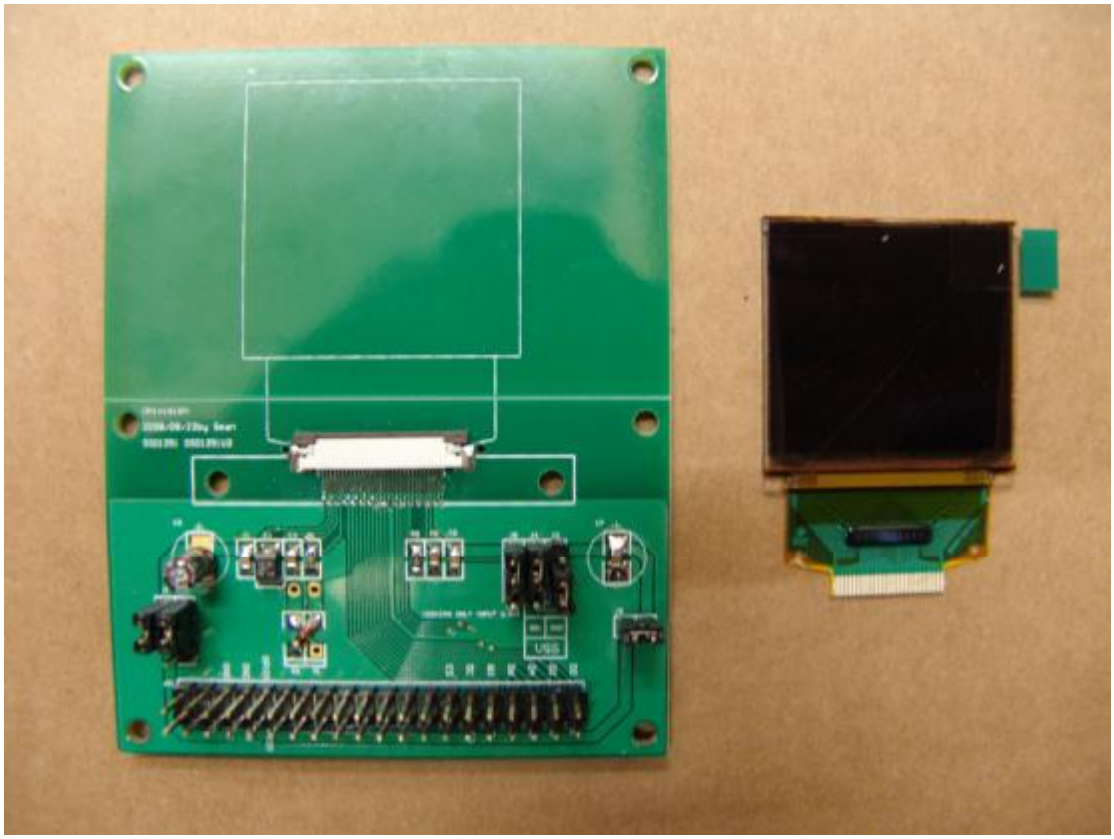


Figure 5 EVK PCB and OLED Module

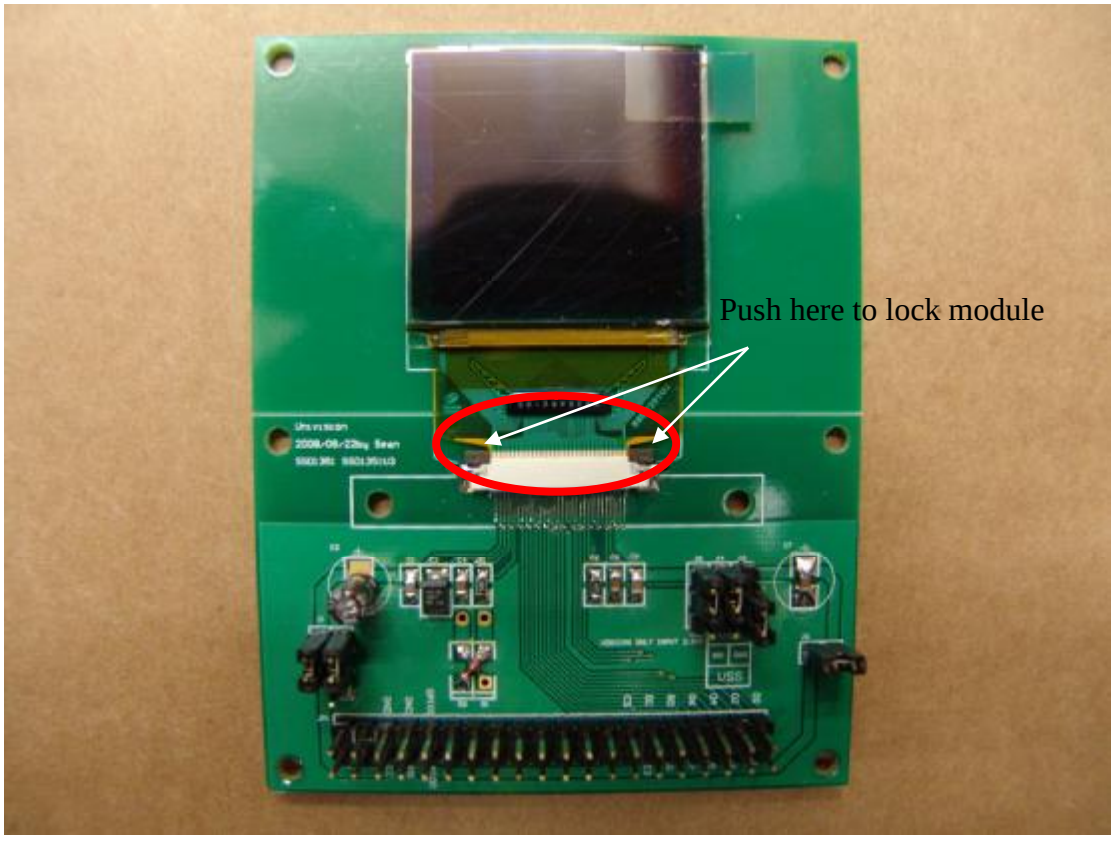


Figure 6 The combination of the module and EVK

Because the package of UG-2828GDEDF11 is COF, that the connect pads are on the top of the module, and the connector which on the EVK PCB board is double size connect type. So when assemble the module with EVK. The module must face up first and plug into the connector. When finished assembled the module and EVK, then push the locking pad to lock the module. See the figure 6.

When finished assembled the module and EVK. User can use leading wire to connect EVK with customer's system. The example shows as figure 7.

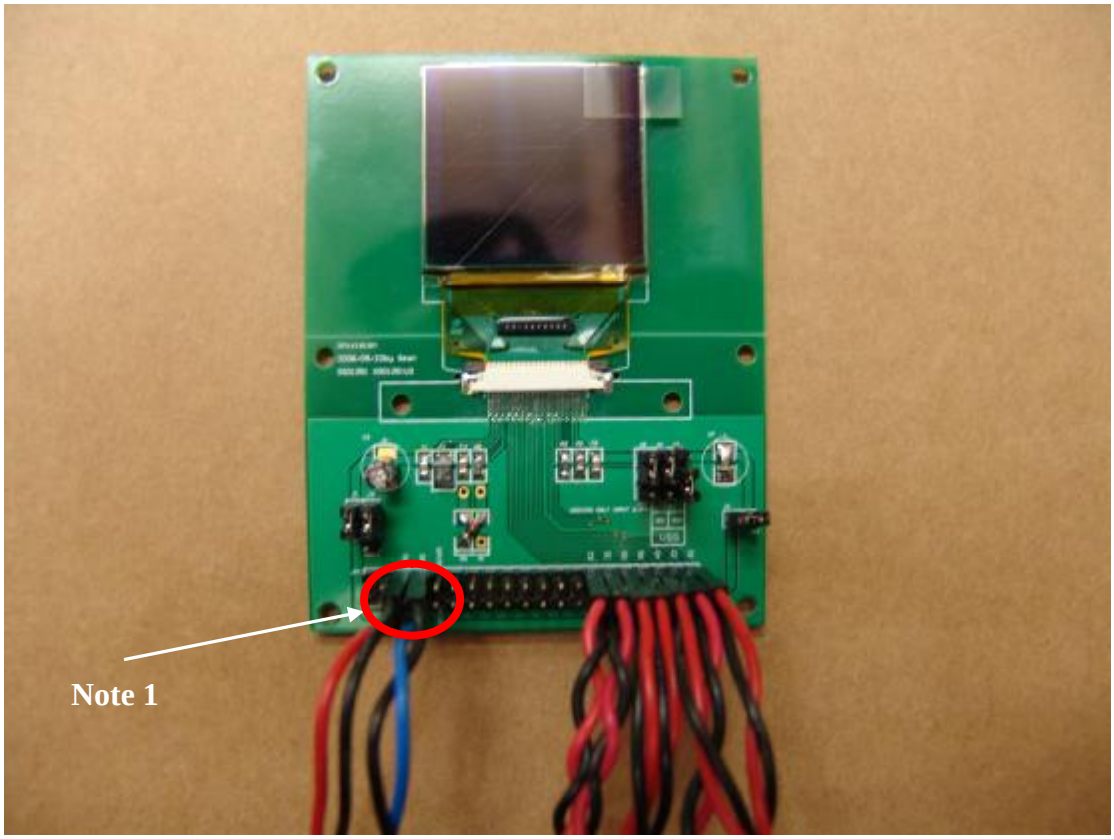


Figure 7 control MCU connect with EVK

Note 1：It is the external most positive voltage supply. In this sample is connected to power supply.

6. Power down and Power up Sequence

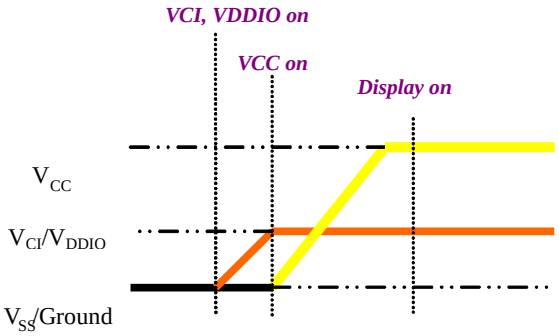
To protect OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

Power up Sequence:

1. Power up V_{CI} & V_{DDIO}
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms

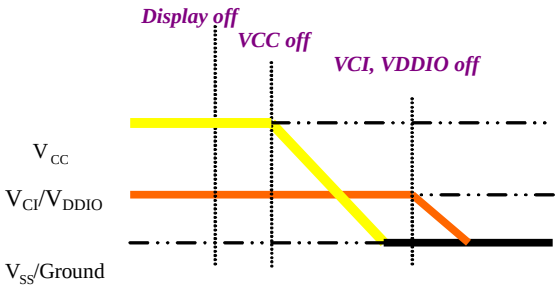
(when V_{CC} is stable)

7. Send Display on command



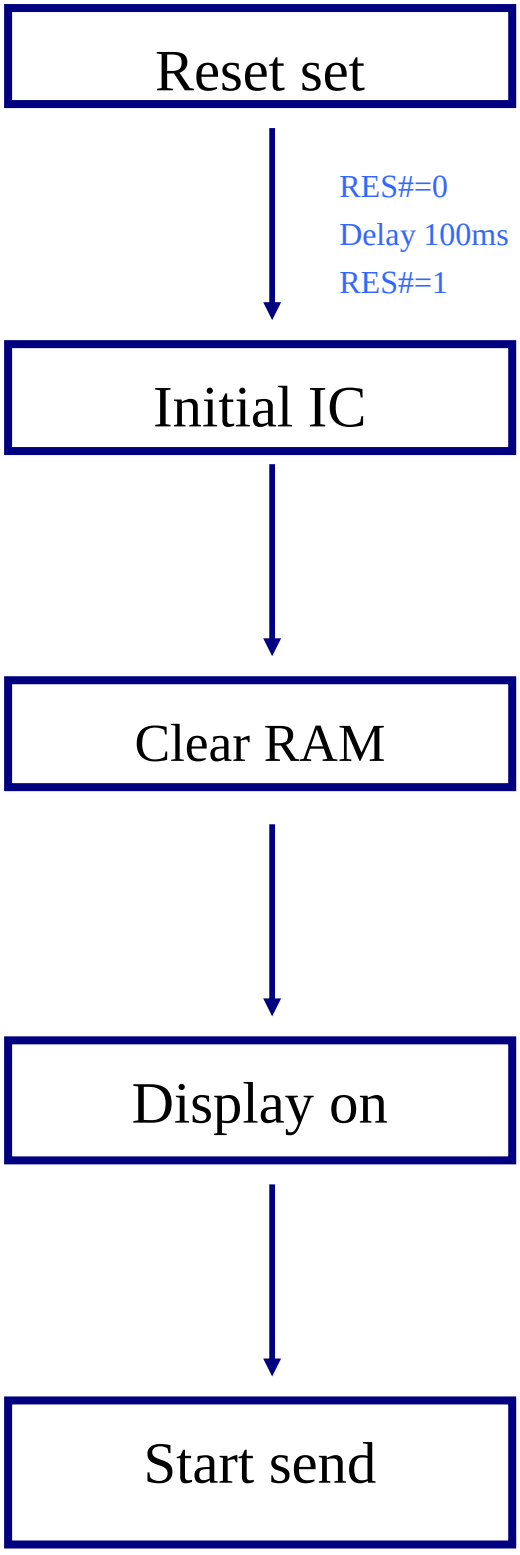
Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
4. Power down V_{CI} & V_{DDIO}



7. How to use SSD1351 module

7.1 Initial Step Flow



7.2 RD recommend Initial Code for 8080 Interface

```
write_c(0xfd);          // Set Command Lock
write_d(0xb1);

write_c(0xae);          // Display off

write_c(0x15);          //set column
write_d(0x00);
write_d(0x7f);

write_c(0x75);          //set row
write_d(0x00);
write_d(0x7f);

write_c(0xa0);          // Set Re-map / Color Depth
write_d(0x74);

write_c(0xa1);          // Set display start line
write_d(0x00);

write_c(0xa2);          // Set display offset
write_d(0x00);

write_c(0xa6);          // Normal display

write_c(0xab);          // Set Function selection
write_d(0x00);

write_c(0xaf);          // Set Sleep mode

write_c(0xb1);          // Set pre & dis_charge
write_d(0x32);

write_c(0xb3);          // clock & frequency
write_d(0xf1);

write_c(0xb4);          // Set Segment LOW Voltage
write_d(0xa0);
write_d(0xb5);
write_d(0x55);

write_c(0xb5);          // Set GPIO
write_d(0x0A);

write_c(0xb6);          // Set Second Pre-charge Period
write_d(0x01);

write_c(0xb8);          //Set Gray Table
write_d(0);             //0
write_d(2);             //1
write_d(3);             //2
write_d(4);             //3
write_d(5);             //4
write_d(6);             //5
write_d(7);             //6
write_d(8);             //7
write_d(9);             //8
write_d(10);            //9
write_d(11);            //10
```

```
write_d(12);          //11
write_d(13);          //12
write_d(14);          //13
write_d(15);          //14
write_d(16);          //15
write_d(17);          //16
write_d(18);          //17
write_d(19);          //18
write_d(21);          //19
write_d(23);          //20
write_d(25);          //21
write_d(27);          //22
write_d(29);          //23
write_d(31);          //24
write_d(33);          //25
write_d(35);          //26
write_d(37);          //27
write_d(39);          //28
write_d(42);          //29
write_d(45);          //30
write_d(48);          //31
write_d(51);          //32
write_d(54);          //33
write_d(57);          //34
write_d(60);          //35
write_d(63);          //36
write_d(66);          //37
write_d(69);          //38
write_d(72);          //39
write_d(76);          //40
write_d(80);          //41
write_d(84);          //42
write_d(88);          //43
write_d(92);          //44
write_d(96);          //45
write_d(100);         //46
write_d(104);         //47
write_d(108);         //48
write_d(112);         //49
write_d(116);         //50
write_d(120);         //51
write_d(125);         //52
write_d(130);         //53
write_d(135);         //54
write_d(140);         //55
write_d(145);         //56
write_d(150);         //57
write_d(155);         //58
write_d(160);         //59
write_d(165);         //60
write_d(170);         //61
write_d(175);         //62
write_d(180);         //63

write_c(0xbb);        // Set pre-charge voltage of color A B C
write_d(0x17);

write_c(0xbe);        // Set VcomH
write_d(0x05);
```

```
        write_c(0xc1);          // Set contrast current for A B C
        write_d(0xc8);
        write_d(0x80);
        write_d(0xc8);

        write_c(0xc7);          // Set master contrast
        write_d(0x0f);

        write_c(0xca);          // Duty
        write_d(0x7f);

        write_c(0xaf);          // Display on
```

7.2.1 Sub Function for 80 Interface

```
void write_c(unsigned char out_command)
{
        DC=0;
        CS=0;
        RW=0;
        P1=out_command;
        RW=1;
        CS=1;
        DC=1;
}

void write_d(unsigned char out_data)
{
        DC=1;
        CS=0;
        RW=0;
        P1=out_data;
        RW=1;
        CS=1;
        DC=0;
}
```

Note：1.For 80 series CPU interface.

2.For 8 Bbit Ttiple Transfer 65K support.